Proceedings of CONF-APMM 2026 Symposium: Quantum Communication and Model Simulation
DOI: 10.54254/2753-8818/2026.GL36229

High-Breakdown-Field β-Ga_2O_3 Power FinFETs on Low Cost Bulk Substrates

Baiyu Chen

College of Science and Engineering, Jinan University, Guangzhou, China
edisonchen@stu2024.jnu.edu.cn

Abstract. β-Ga_2O_3 has emerged as a promising ultrawide-bandgap semiconductor for next-generation high-voltage power electronics because of its large bandgap, high critical electric field and potential compatibility with low-cost bulk substrates. This review systematically examines recent progress in vertical β-Ga_2O_3 power FinFETs, with emphasis on device physics, electrostatic design, epitaxial growth, fin patterning and thermal management. This article summarizes how three-dimensional gate control and fin geometry enable enhancement-mode operation without relying on p-type doping and compares reported device performance in terms of threshold behavior, breakdown strength and voltage scalability. The review also highlights the complementary roles of HVPE and MOCVD in realizing thick drift layers and low-doped channel regions, as well as the importance of low-damage dry etching in preserving fin sidewall integrity and electrostatic control. Finally, the major limitation of self-heating is discussed together with practical mitigation strategies, including heterogeneous integration, backside heat extraction and interface passivation. Overall, vertical β-Ga_2O_3 FinFETs represent a compelling route toward ultrahigh-voltage power devices, but their practical deployment will depend on coordinated advances in materials growth, process optimization and thermal management.

Keywords: β-Ga_2O_3, vertical FinFET, ultrawide-bandgap semiconductors, thermal management

1. Introduction

The global momentum toward transportation electrification, renewable energy grid integration and high-efficiency power conversion systems has engendered an urgent demand for semiconductor materials capable of reliable operation under high-voltage, high-current, and high-temperature conditions while exhibiting minimal energy dissipation. Power semiconductor devices are the key building blocks of modern energy conversion systems, serving critical roles in electric vehicles, renewable energy infrastructure, smart grids, and aerospace applications. Among these, vertical-structure devices, through judicious engineering of their voltage sustaining drift layers, can simultaneously achieve kilovolt level breakdown voltages and kiloampere level current ratings per unit chip area, rendering them ideally suited for applications that demand ultra high power density, superior efficiency and compact form factors.

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Owing to its well-established manufacturing infrastructure and inherent cost benefits, silicon (Si) has long dominated the power electronics landscape. However, its relatively narrow bandgap of 1.1 eV and low critical electric field of 0.3 MV/cm impose fundamental limits on achievable breakdown voltage and operating temperature, thereby constraining system efficiency and power density [1]. These limitations have driven intensive interest in wide-bandgap semiconductors among which β-Ga_2O_3 is particularly attractive because of its 4.9 eV bandgap, 8 MV/cm theoretical critical field, potential compatibility with low-cost bulk substrates and higher Baliga figure of merit compared to those of SiC and GaN [2, 3]. Its extremely low intrinsic carrier concentration (10^{-23} cm^{-3} at room temperature) further suggests low-leakage operation at elevated temperatures [4].

Over the past decade, β-Ga_2O_3 power transistors have evolved from early proof-of-concept devices to kilovolt-class lateral and vertical architectures, demonstrating the strong potential of this material system for ultrahigh-voltage applications. In parallel with these voltage-scaling achievements, several device architectures, including lateral MOSFETs, MESFETs, trench structures and vertical devices, have been explored to better exploit the intrinsic material advantages of β-Ga_2O_3.

Despite this progress, two intrinsic limitations continue to hinder practical deployment: the difficulty of achieving reliable p-type doping and the low thermal conductivity of the material. The former limits conventional p–n junction design and complicates enhancement-mode operation, while the latter aggravates self-heating and degrades long-term device reliability under high power density [5]. As a result, the practical development of β-Ga_2O_3 power devices depends not only on material quality, but also on device architecture, epitaxial growth, processing fidelity and thermal management. In this context, vertical FinFETs have attracted growing attention because their three-dimensional gate electrostatics can provide strong channel control and enable enhancement-mode operation without relying on p-type doping.

This review summarizes recent progress in vertical β-Ga_2O_3 power FinFETs from four perspectives: device physics and electrostatic design, epitaxial growth and fabrication processes, representative performance metrics and thermal management strategies. The remainder of this paper is organized as follows. Section II reviews the device structure and operating principles. Section III summarizes epitaxy and fabrication technologies. Section IV discusses key challenges and mitigation strategies and Section V concludes the paper with an outlook on future research directions.

2. Device design: vertical β-Ga_2O_3 FinFETs

2.1. Vertical device structure

The fundamental obstacle to realizing practical power devices in β-Ga_2O_3 lies in its severe doping asymmetry. As shown in figure. 1, the conduction band minimum (CBM) of β-Ga_2O_3 lies at approximately 4.0 eV below the vacuum level, whereas the valence band maximum (VBM) is as deep as approximately 8.8 eV and the Fermi level (E_f) is pinned close to the CBM [6]. This band-edge configuration reflects the intrinsically n-type nature of β-Ga_2O_3 and makes acceptor activation highly unfavorable.

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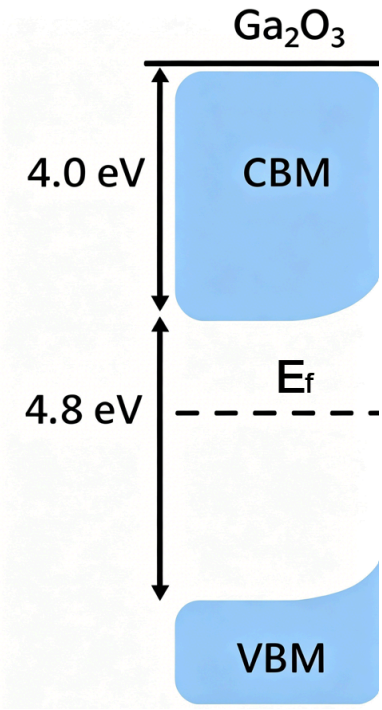

Figure 1. Energy band diagram of Ga_2O_3

In contrast to SiC and GaN where acceptor impurities such as Al and Mg introduce shallow levels with ionization energies of merely 0.2 eV and 0.17eV respectively, the VBM of β-Ga_2O_3 lies unusually deep, so that any candidate acceptor either settles into a deep polaronic states with ionization energies exceeding 1.3 eV or become resonant within the valence band. Compounding this thermodynamic barrier, strong Fröhlich electron–phonon coupling causes holes self-trap spontaneously into small polarons, rendering them nearly immobile. Taken together, these thermodynamic and kinetic barriers make heavy p-type doping unattainable no matter which dopant species one attempts.

To circumvent this bottleneck, a vertical FinFET architecture has been proposed in recent studies, where strong three-dimensional electrostatic control enables normally-off operation without relying on p-type doping, which is shown in figure.2.

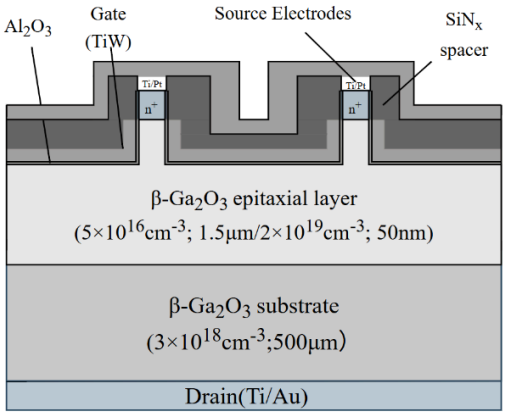

Figure 2. Schematic structure of the vertical β-Ga_2O_3 FinFET

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The vertical configuration is preferentially selected over lateral designs to fully exploit the ultra-wide bandgap (4.8 eV) and the superior breakdown characteristics of β-Ga_2O_3 for high-voltage/high-current power applications. From bottom to top, the device consists of a highly conductive β-Ga_2O_3 substrate with a doping concentration of 3×10^{18} cm^{-3}, followed by an epitaxially grown drift/channel layer with a doping concentration of 5×10^{16} cm^{-3} [7]. The epitaxial layer includes a 1.5 μm drift region and a 50 nm channel region. Fin structures are subsequently defined by electron beam lithography and dry etching processes. The gate stack comprises a TiW gate metal and an Al_2O_3 gate dielectric, while SiNx spacers are formed through photoresist planarization followed by self-aligned etching. Finally, source electrodes are fabricated on top of the fin structures, whereas the drain electrode (TiW/Au) is deposited on the backside of the substrate, thereby establishing the vertical current conduction path.

2.2. Operating principles and electrostatic design

The tri-gate FinFET architecture wraps the gate around a narrow fin channel, thereby strengthening electrostatic control and enabling complete channel depletion in the off state. In β-Ga_2O_3 FinFETs, enhancement-mode operation is primarily achieved through geometric and electrostatic optimization rather than solely by aggressively reducing the doping concentration. The principal design parameters include the fin width (W_{FIN}), donor concentration (N_d), gate metal work function, dielectric constant and the unintentional interface charge density at the β-Ga_2O_3/dielectric interface.

Simulation results reported in [7] demonstrate that the fin width, drift-region doping concentration and gate metal work function collectively govern the threshold voltage and enhancement-mode characteristics of β-Ga_2O_3 FinFETs. For a fixed fin width, lowering the donor concentration facilitates complete depletion of the channel. Nevertheless, both simulation and experimental results indicate that stable enhancement-mode operation can still be achieved at a relatively high doping concentration (on the order of 5×10^{16} cm^{-3}), provided that the fin width is sufficiently reduced and an appropriate gate work function is selected. In essence, the three-dimensional gate surrounding the narrow fin channel imposes strong electrostatic confinement.

2.3. Key performance metrics

The vertical β-Ga_2O_3 FinFET architecture naturally supports enhancement-mode (normally-off) operation, making it attractive for fail-safe power electronics. In 2023, Tetzner et al. reported enhancement-mode operation in vertical (100) β-Ga_2O_3 FinFETs with a positive threshold voltage of +4.2 V and an on/off current ratio of 10^5. Three-terminal off-state breakdown measurements revealed catastrophic breakdown at 260 V, yielding an average breakdown field of 2.7 $MV \cdot cm^{-1}$. These figures exceeded what has been reported for vertical SiC- and GaN-based power transistors, pointing to the promise of vertical β-Ga_2O_3 FinFETs in next-generation high-voltage power applications. Device simulations further revealed pronounced electric-field crowding near the gate edge outside the active region, with the peak fields reaching 7 $MV \cdot cm^{-1}$ in the Al_2O_3 gate dielectric and 5 $MV \cdot cm^{-1}$ in the β-Ga_2O_3 semiconductor [7].

3. Epitaxy and fabrication technology

High-performance FinFET fabrication relies on the coordinated development of advanced epitaxial growth and precision microfabrication technologies. From the perspective of material growth, hydride vapor phase epitaxy (HVPE) is adopted for forming the thick drift layers required for ultra-

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high-voltage operation, whereas metal-organic chemical vapor deposition (MOCVD) is preferred for channel layers with high crystalline quality to support efficient carrier transport. On device fabrication side, dry etching defines fin structures with critical dimensions down to 350 nm, ensuring effective electrostatic control through aggressive dimensional scaling. High-performance β-Ga_2O_3 FinFETs ultimately rest on the joint optimization of epitaxial growth and fabrication processes.

3.1. Halide vapor phase epitaxy (HVPE)

HVPE has become the workhorse for thick, lightly doped β-Ga_2O_3 drift layers, especially where high-voltage devices demand both high throughput and wafer-scale scalability. Its high growth rate enables rapid deposition of thick epitaxial layers, and its compatibility with large-diameter substrates aligns well with the throughput requirements of commercial manufacturing. For ultra-high-voltage β-Ga_2O_3 devices, these advantages make HVPE hard to replace.

For vertical β-Ga_2O_3 FinFETs targeting breakdown voltages above 1 kV, the thick drift layer grown by HVPE satisfies the requirement. After drift-layer growth, a MOCVD-grown channel layer is typically introduced, achieving background doping concentrations $\leq 1 \times 10^{16}$ cm^{-3}—a prerequisite for complete depletion of the fin channel and the positive threshold voltage that defines enhancement-mode operation. Rather than being rival techniques, HVPE and MOCVD each handle a distinct set of process requirements within the same fabrication sequence.

3.2. Metal-organic chemical vapor deposition (MOCVD)

MOCVD is primarily employed for channel-layer growth in β-Ga_2O_3 FinFET fabrication. Its atomic-level control over doping profiles is essential for tailoring the properties of both the channel and drift regions. Compared with HVPE, MOCVD enables finer control over composition and dopant distribution, making it particularly valuable for channel engineering and interface-sensitive device stacks.

3.3. Dry etching for nanoscale fin fabrication

Fabricating sub-micrometer fin structures with near-vertical sidewalls remains one of the hardest steps in β-Ga_2O_3 FinFET processing. Unlike planar MOSFETs, where the conductive channel is confined to a single interface, current conduction in tri-gate FinFETs extends along the entire fin sidewall. This means plasma-induced sidewall damage cuts deeper into device performance. Ion bombardment generates oxygen vacancies at the surface, leading to the formation of positively charged donor-like trap states. These defects degrade carrier mobility via Coulomb scattering. They also cause a negative shift in threshold voltage and in the worst case can wipe out enhancement-mode operation entirely.

Dry etching techniques have achieved significant progress to cope with the challenge. It demonstrated the capability to fabricate fins as narrow as 350 nm with near-vertical sidewalls (sidewall angles > 85°) while the low-damage etching processes minimize surface roughness which is critical for reducing interface trap density and ensuring uniform gate control. In addition, the technique supports high-aspect-ratio fin structures necessary for vertical device geometries. The etching process must be carefully optimized to balance etch rate, selectivity to mask materials and surface damage. Post-etch surface treatments including wet cleaning and annealing are essential to remove etch-induced damage and prepare the surface for gate dielectric deposition.

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The realization of vertical β-Ga_2O_3 FinFETs is predicated upon a precise reconciliation of epitaxial film quality with etching fidelity. Notwithstanding near-ideal material characteristics and device geometries, the intrinsically low thermal conductivity of β-Ga_2O_3 establishes a fundamental upper bound on the practically attainable current rating. This thermal constraint has accordingly redirected the research emphasis from front-end process optimization to back-end thermal packaging methodologies.

4. Key challenges and strategy

β-Ga_2O_3 has several useful material advantages, especially a high breakdown electric field and the possibility of relatively low-cost substrate growth. These properties make it attractive for high-voltage power devices. In practical field-effect transistors, however, device performance is governed by factors beyond intrinsic material parameters. The device also needs to keep stable electrical behavior under high voltage, high current density and long operation time.

4.1. Self-heating

A clear weakness of β-Ga_2O_3 is its low thermal conductivity compared with SiC and GaN. In a power FET, heat is mainly generated near the channel region, where current density and electric field are high. Since the heat does not dissipate efficiently, a local hotspot can form in the active device region. As the channel temperature rises, carrier mobility decreases, so the specific on-resistance increases and conduction loss becomes larger. The high local temperature may also accelerate degradation of gate dielectrics, metal contacts and interface states. In spite of the fact that β-Ga_2O_3 can support high breakdown voltage in theory, poor heat dissipation can limit the usable power density in practice.

4.2. Thermal management strategy

The thermal problem cannot be solved by adjusting a single parameter alone. A more realistic solution is to combine material integration, device layout and package-level cooling. One common method is to use high-thermal-conductivity materials such as diamond, SiC or AlN as heat-spreading layers. Diamond is especially useful because it can remove heat from the channel region more effectively than β-Ga_2O_3 itself [8].

Another approach is heterogeneous integration. For example, a thin β-Ga_2O_3 layer can be transferred or bonded onto a substrate with superior thermal properties, thereby reducing the thermal resistance from the active region to the heat sink and improveing the heat removal path [9]. In addition, backside cooling, metal heat spreaders and package design also affect the final device temperature.

The advantage of β-Ga_2O_3 becomes more meaningful in the range of about 3.3 kV to above 10 kV. Thus, while β-Ga_2O_3 is unlikely to replace SiC or GaN across all voltage classes, its strongest competitiveness is expected in the ultrahigh-voltage regime, where its exceptional breakdown field can translate into thinner drift layers, smaller device area and potentially lower conduction loss.

Future progress will depend less on the intrinsic material advantage alone than on the co-optimization of epitaxy, interface engineering, thermal extraction and long-term reliability. In this sense, device commercialization will be determined by system integration rather than by a single performance metric.

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5. Conclusion

This review has systematically surveyed the device physics, fabrication technologies, thermal management challenges and corresponding mitigation strategies of β-Ga_2O_3 field-effect transistors. Recent experimental results and reported literature indicate that gate-engineered device architectures have largely mitigated the long-standing challenge associated with the absence of p-type doping in β-Ga_2O_3, making it a promising platform for high-voltage power electronics. On the fabrication front, advances in HVPE, MOCVD and dry etching have enabled large-area homoepitaxial growth and high-precision device patterning on low-cost bulk substrates. Yet the intrinsically low thermal conductivity of β-Ga_2O_3 continues to constrain its commercial viability. Addressing this challenge will require coordinated development of thermal-management schemes, heterogeneous integration platforms, backside cooling architectures and robust surface/interface passivation protocols.

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